

Exam

Name \_\_\_\_\_

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

- 1) A LOW input to an inverter produces a HIGH output. 1) \_\_\_\_\_  
Answer:  True  False
- 2) The OR gate performs a function similar to series-connected switches. 2) \_\_\_\_\_  
Answer:  True  False
- 3) The output of an AND gate is HIGH only when all inputs are HIGH. 3) \_\_\_\_\_  
Answer:  True  False
- 4) The output of an AND gate is LOW only when all inputs are LOW. 4) \_\_\_\_\_  
Answer:  True  False
- 5) When the inputs to a 3-input AND gate are 001, the output is HIGH. 5) \_\_\_\_\_  
Answer:  True  False
- 6) When the inputs to a 3-input OR gate are 001, the output is HIGH. 6) \_\_\_\_\_  
Answer:  True  False
- 7) The output of an OR gate is HIGH when at least one input is HIGH. 7) \_\_\_\_\_  
Answer:  True  False
- 8) The output of an OR gate is LOW when at least one input is LOW. 8) \_\_\_\_\_  
Answer:  True  False
- 9) The output of a NAND gate is HIGH only when one or more inputs are HIGH. 9) \_\_\_\_\_  
Answer:  True  False
- 10) The output of a NAND gate is LOW only when all inputs are HIGH. 10) \_\_\_\_\_  
Answer:  True  False
- 11) The output of a NOR gate is LOW only when all inputs are HIGH. 11) \_\_\_\_\_  
Answer:  True  False
- 12) The output of a NOR gate is HIGH only when all inputs are HIGH. 12) \_\_\_\_\_  
Answer:  True  False
- 13) When the inputs to a 3-input NAND gate are 001, the output is HIGH. 13) \_\_\_\_\_  
Answer:  True  False
- 14) When the inputs to a 3-input NOR gate are 001, the output is LOW. 14) \_\_\_\_\_  
Answer:  True  False

15) The output of a 2-input Exclusive-OR gate is HIGH when the inputs are equal, or identical. 15) \_\_\_\_\_

Answer: True  False

16) The output of a 2-input Exclusive-NOR gate is HIGH when the inputs are equal, or identical. 16) \_\_\_\_\_

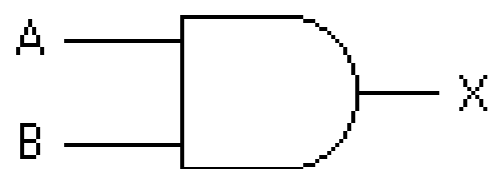
Answer:  True  False

17) A circle, or "bubble," on a distinctive-shape logic symbol indicates a logic inversion. 17) \_\_\_\_\_

Answer:  True  False

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

18) The symbol below represents a(n) \_\_\_\_\_. 18) \_\_\_\_\_



A) NAND gate

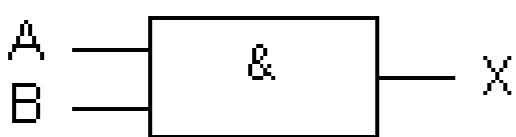
C) OR gate

B) AND gate

D) none of the above

Answer: B

19) The symbol below represents a(n) \_\_\_\_\_. 19) \_\_\_\_\_



A) NAND gate

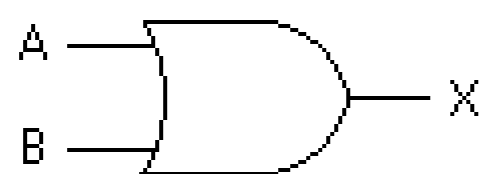
C) OR gate

B) AND gate

D) none of the above

Answer: B

20) The symbol below represents a(n) \_\_\_\_\_. 20) \_\_\_\_\_



A) AND gate

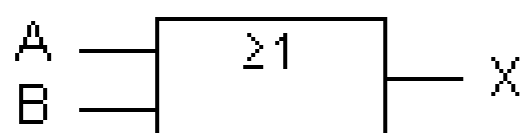
C) OR gate

B) Inverter

D) none of the above

Answer: C

21) The symbol below represents a(n) \_\_\_\_\_. 21) \_\_\_\_\_



A) Inverter

C) AND gate

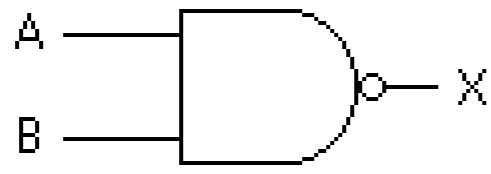
B) OR gate

D) none of the above

Answer: B

22) The symbol below represents a(n) \_\_\_\_\_.

22) \_\_\_\_\_

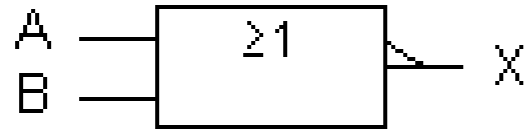


- A) OR gate                      B) Inverter                      C) AND gate                      D) NAND gate

Answer: D

23) The symbol below represents a(n) \_\_\_\_\_.

23) \_\_\_\_\_

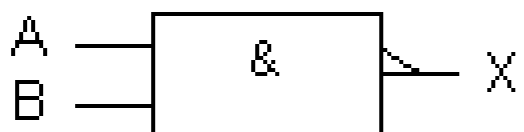


- A) Exclusive-NOR gate                      B) inverter  
C) NOR gate                      D) NAND gate

Answer: C

24) The symbol below represents a(n) \_\_\_\_\_.

24) \_\_\_\_\_

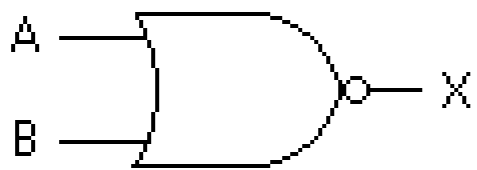


- A) NOR gate                      B) NAND gate  
C) inverter                      D) Exclusive-NOR gate

Answer: B

25) The symbol below represents a(n) \_\_\_\_\_.

25) \_\_\_\_\_

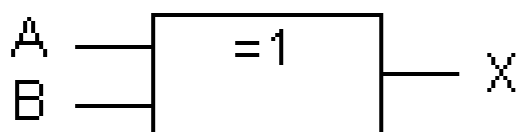


- A) AND gate                      B) NAND gate                      C) NOR gate                      D) OR gate

Answer: C

26) The symbol below represents a(n) \_\_\_\_\_.

26) \_\_\_\_\_

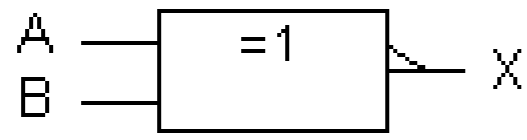


- A) OR gate                      B) Exclusive-OR gate  
C) NAND gate                      D) AND gate

Answer: B

27) The symbol below represents a(n) \_\_\_\_\_.

27) \_\_\_\_\_



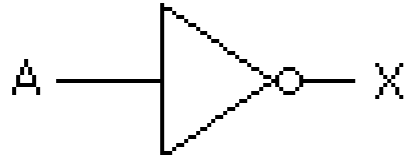
- A) Exclusive-NOR gate
- C) NAND gate

- B) Exclusive-OR gate
- D) NOR gate

Answer: A

28) The symbol below represents a(n) \_\_\_\_\_.

28) \_\_\_\_\_



- A) Inverter

- B) OR gate

- C) AND gate

- D) NAND gate

Answer: A

29) The truth table below describes a(n) \_\_\_\_\_.

29) \_\_\_\_\_

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

- A) AND gate

- B) OR gate

- C) NOR gate

- D) NAND gate

Answer: A

30) The truth table below describes a(n) \_\_\_\_\_.

30) \_\_\_\_\_

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

- A) AND gate

- B) OR gate

- C) NOR gate

- D) NAND gate

Answer: B

31) The truth table below describes a(n) \_\_\_\_\_.

31) \_\_\_\_\_

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

- A) AND gate

- B) OR gate

- C) NOR gate

- D) NAND gate

Answer: D

32) The truth table below describes a(n) \_\_\_\_\_.

32) \_\_\_\_\_

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

- A) AND gate                      B) OR gate                      C) NOR gate                      D) NAND gate

Answer: C

33) Which of the truth tables below describes the Exclusive-NOR gate?

33) \_\_\_\_\_

A	B	X	A	B	X	A	B	X	A	B	X
0	0	1	0	0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	1	1	0	1	0
1	0	0	1	0	1	1	0	1	1	0	0
1	1	1	1	1	0	1	1	0	1	1	0

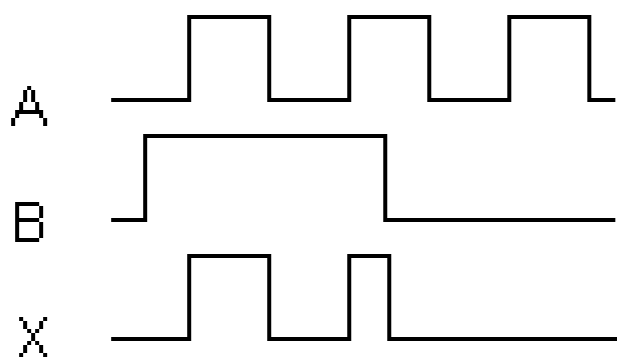
- (A)                      (B)                      (C)                      (D)

- A) (A)                      B) (B)                      C) (C)                      D) (D)

Answer: A

34) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate.

34) \_\_\_\_\_

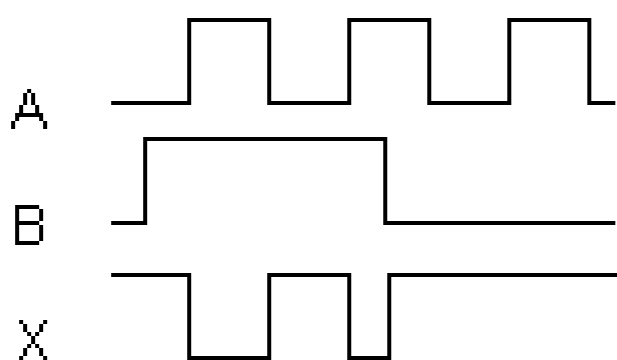


- A) AND                      B) OR                      C) NAND                      D) Exclusive-OR

Answer: A

35) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate.

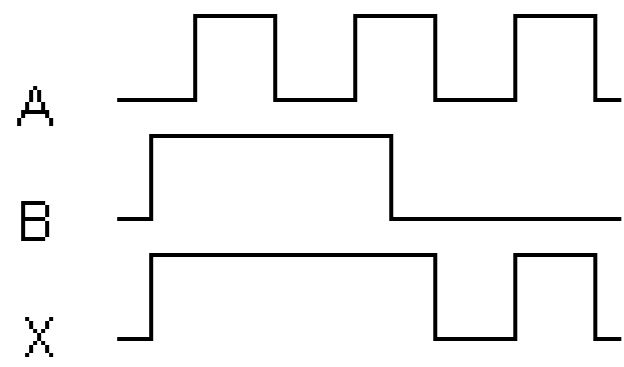
35) \_\_\_\_\_



- A) AND                      B) OR                      C) NAND                      D) Exclusive-OR

Answer: C

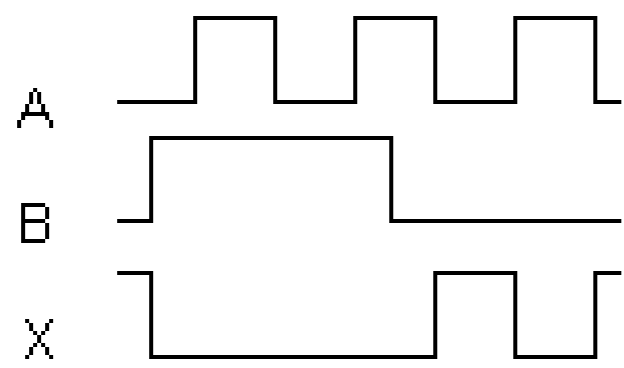
36) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate. 36) \_\_\_\_\_



- A) AND                      B) OR                      C) NAND                      D) Exclusive-OR

Answer: B

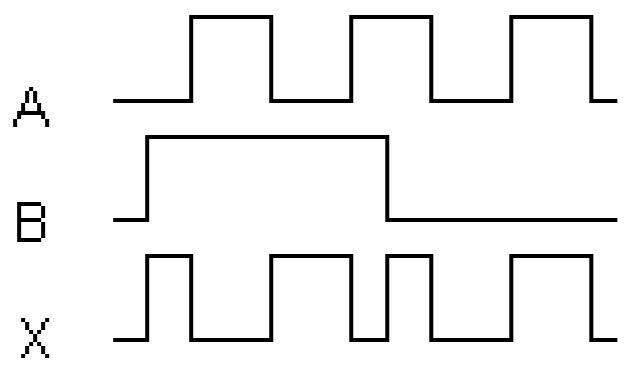
37) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate. 37) \_\_\_\_\_



- A) AND                      B) OR                      C) Exclusive-NOR                      D) NOR

Answer: D

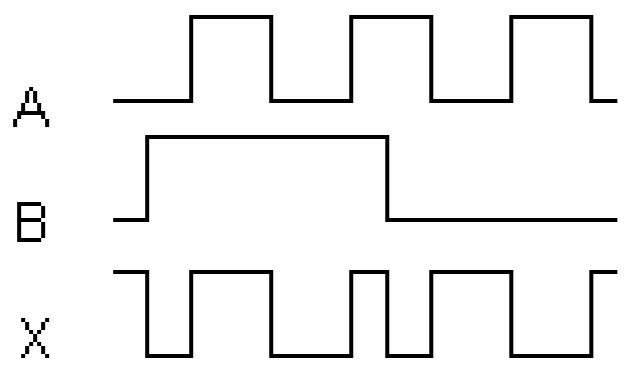
38) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate. 38) \_\_\_\_\_



- A) NAND                      B) Exclusive-NOR                      C) AND                      D) Exclusive-OR

Answer: D

39) The timing diagram below is correct for a 2-input \_\_\_\_\_ gate. 39) \_\_\_\_\_



- A) Exclusive-OR                      B) NAND                      C) AND                      D) Exclusive-NOR

Answer: D

40) IC's with a \_\_\_\_\_ prefix have a broad operating temperature range and are generally used by the military. 40) \_\_\_\_\_

- A) 74                      B) TTL                      C) 2N                      D) 54

Answer: D

- 41) The \_\_\_\_\_ series of IC's are pin, function and voltage-level compatible with the 74 series IC's. 41) \_\_\_\_\_  
 A) ALS                                      B) 2N                                      C) HCT                                      D) CMOS  
 Answer: C
- 42) A logic gate draws 10mA when its output is HIGH and 20mA when its output is LOW. When operating from a 12V supply with a 10% duty cycle the average power dissipation will be \_\_\_\_\_. 42) \_\_\_\_\_  
 A) 228mW                                      B) 360mW                                      C) 324mW                                      D) 180mW  
 Answer: A
- 43) The fanout for standard bipolar logic devices is \_\_\_\_\_. 43) \_\_\_\_\_  
 A) 5                                      B) 10                                      C) 2                                      D) 1  
 Answer: B
- 44) The term "hex inverter" refers to \_\_\_\_\_. 44) \_\_\_\_\_  
 A) six inverters in a single package                                      B) an inverter which has six inputs  
 C) an inverter that has a history of failure                                      D) a six-input symbolic logic device  
 Answer: A
- 45) Which type of gate can be used to add two bits? 45) \_\_\_\_\_  
 A) XNAND                                      B) NOR                                      C) NAND                                      D) XOR  
 Answer: D
- 46) An AND gate is checked for operation and the following readings are taken on the gate: input A = 0.2 V, input B = 4.5 V, input C = 0.4 V, output = 4.9 V. What might be wrong with the gate? 46) \_\_\_\_\_  
 A) Input C is too high.                                      B) The output is stuck high; the chip is bad.  
 C) The output is too low: it should be 5 V.                                      D) Nothing is wrong with the gate.  
 Answer: B
- 47) When an open occurs on the input to a bipolar logic device, the output will \_\_\_\_\_. 47) \_\_\_\_\_  
 A) go LOW, because there is no current in an open circuit  
 B) go HIGH, since full voltage appears across an open  
 C) react to the open input as if it were a HIGH input  
 D) still be good, if only the good inputs are used  
 Answer: C
- 48) When an open occurs on the input of a CMOS gate, the output will \_\_\_\_\_. 48) \_\_\_\_\_  
 A) go LOW, because there is no current in an open circuit  
 B) go HIGH, since full voltage appears across an open  
 C) be treated as if the open input were a HIGH  
 D) be unpredictable; it may go HIGH or LOW  
 Answer: D
- 49) What technology allows a GAL to be reprogrammed again and again? 49) \_\_\_\_\_  
 A) TTL                                      B) CMOS                                      C) E2CMOS                                      D) NMOS  
 Answer: C

- 50) What programmable arrays are in PLD's? 50) \_\_\_\_\_  
 A) OR arrays and AND arrays B) OR arrays only  
 C) AND arrays only D) NOR arrays  
 Answer: A
- 51) Which of the following is not a type of SPLD? 51) \_\_\_\_\_  
 A) GAL B) RAM C) PLA D) PROM  
 Answer: B
- 52) The difference between a PLA and a PAL is \_\_\_\_\_. 52) \_\_\_\_\_  
 A) the PAL has more possible product terms than the PLA  
 B) the PLA has a programmable OR plane and a programmable AND plane while the PAL only has a programmable AND plane  
 C) the PAL has a programmable OR plane and a programmable AND plane while the PLA only has a programmable AND plane  
 D) PALs and PLAs are the same thing.  
 Answer: B
- 53) HDL stands for \_\_\_\_\_. 53) \_\_\_\_\_  
 A) hardware descriptive logic B) hardware description language  
 C) hardwired digital logic D) none of the above  
 Answer: B
- 54) HDLs differ from \_\_\_\_\_ in that they include ways of describing propagation times and other logic characteristics. 54) \_\_\_\_\_  
 A) software programming languages B) software digital logic  
 C) software description languages D) none of the above  
 Answer: C
- 55) The \_\_\_\_\_ in a VHDL program defines the logic element and its inputs/outputs or ports. 55) \_\_\_\_\_  
 A) source B) hardware C) entity D) architecture  
 Answer: C
- 56) The \_\_\_\_\_ in a VHDL program describes its logic operation. 56) \_\_\_\_\_  
 A) source B) architecture C) entity D) hardware  
 Answer: B
- 57) A \_\_\_\_\_ IC comes with logic functions that are not programmed in and cannot be altered. 57) \_\_\_\_\_  
 A) VHDL B) HDL C) fixed-function D) microcontroller  
 Answer: C